SEMICONDUCTOR STORAGE DEVICE AND REFRESH METHOD FOR THE SAME

ABSTRACT

[0076] A DRAM capable of inserting a refresh operation during an ordinary access operation and setting the internal cycle time longer than half the external cycle time. An address selector selects an access row address signal ERA or a refresh row address signal RRA. A row decoder control circuit selects one of several divided blocks of a memory cell array in response to the selected row address signal RA, and selects word lines by a row decoder circuit. When the operation starts at one of the blocks, a busy signal/BUSY is activated to inhibit selection performed by the address selector. When the operation ends, the busy signal/BUSY is deactivated to cancel the inhibition of selection by the address selector. Therefore, the row address signal ERA or RRA input earlier acts with priority and the row address signal RRA or ERA subsequently input is made to wait until the preceding operation ends.